(54) ELECTROSTATIC BREAKDOWN PREVENTIVE CIRCUIT IN SEMICONDUCTOR DEVICE AND FORMATION THEREOF

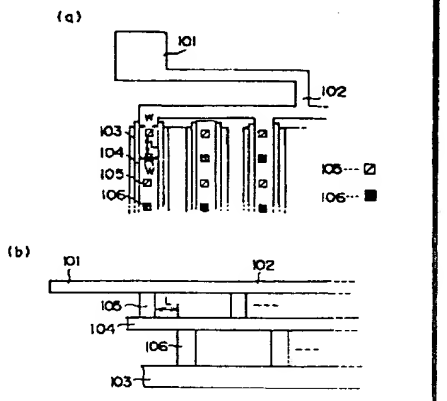
(11) 6-232345 (A) (43) 19.8.1994 (19) JP
(21) Appl. No. 4-186989 (22) 14.7.1992

(71) OKI ELECTRIC IND CO LTD (72) HIDEYUKI ANDO(1)

(51) Int. Cl⁵. H01L27/04

PURPOSE: To provide an electrostatic breakdown preventive circuit in a semiconductor device of a structure, wherein while a sufficient resistance component of voltage drop to charge due to static electricity is kept, a wiring resistance in the whole circuit is made small and a reduction in a chip size is also made possible, and a method of forming the circuit.

CONSTITUTION: A source/drain part 103 of an output transistor is formed on a silicon single crystal semiconductor substrate, then, contact holes 106, which make, a high-resistance wiring layer 104 connect with the part 103 of the transistor, are opened by a photolithography/etching technique and after that, the layer 104 is formed. Contact holes 105 are opened and an output pad 101 and an at aluminum wiring 102 are formed. The constituent elements to obtain a resistance of a voltage drop component as an electrostatic breakdown preventive circuit are the sheet resistivity of the layer 104, the diameters of the contact holes 105 and 106 and the interval between the contact holes 103 and 104 and these three elements are combined with one another.



101: (a pad part)

(54) SEMICONDUCTOR INTEGRATED CIRCUIT AND COMMUNICATIONS DEVICE

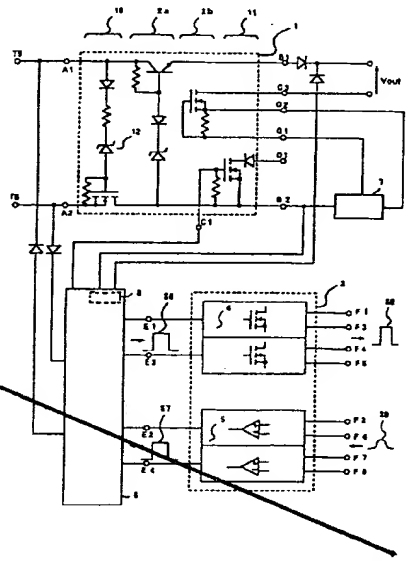
(11) 6-232347 (A) (43) 19.8.1994 (19) JP
(21) Appl. No. 5-14925 (22) 1.2.1993

(71) HITACHI LTD (72) SHIGEYUKI KAWABATA(3)

(51) Int. Cl⁵. H01L27/04

PURPOSE: To prevent a plurality of pieces of block circuits formed on the same chip from being affected by other circuits by a method wherein in the case where any one of the low-breakdown strength block circuits function, the functions of the high-breakdown strength block circuits are stopped.

CONSTITUTION: At the time of operation of a low-breakdown strength block circuit 3, a voltage lower than a Zener voltage in a Zener diode 12 is applied to power-supply receiving terminals A1 and A2 of a high-breakdown strength block circuit 1 by a control from the outside or such a voltage as a potential in the terminal A2 is higher than that in the terminal A1 is applied. Thereby, the function of the circuit 1 is stopped and the circuit 3 can lessen the effect of noise or the like from the circuit 1 and a high-accuracy signal processing can be executed.



6: peripheral circuit, 7: current detector, 8: power supply

(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

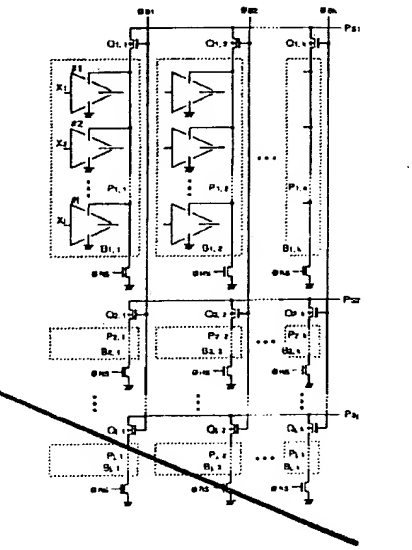
(11) 6-232348 (A) (43) 19.8.1994 (19) JP
(21) Appl. No. 5-15236 (22) 2.2.1993

(71) HITACHI LTD (72) TAKESHI SAKATA(2)

(51) Int. Cl⁵. H01L27/04,H01L21/82,H01L27/10

PURPOSE: To reduce a through current, which is made to flow through a word driver, a decoder and the like, by a method wherein a semiconductor integrated circuit device has column wires arranged in such a way as to cross a plurality of row wires and a plurality of circuit blocks, a necessary voltage is fed to a selected specified circuit block through the wires arranged in a column and a row and a feed of the necessary voltage is stopped to the other circuit blocks.

CONSTITUTION: A necessary word voltage V_{CH} is applied to a row wire P_{S1} to correspond to a B_1·$_1$ and a voltage 0V is applied to a column wire ϕ_{B1} to correspond to the B_1·$_1$. A block selecting P-MOS transistor Q_1·$_1$ is turned ON and a feeder P_1·$_1$ belonging to the B_1·$_1$ is charged with a voltage Vch. A gate voltage of a P-MOS transistor constituting a word driver belonging to the B_1·$_1$ is definite and the Vch is charged in a selected word line. After the P_1·$_1$ is applied the voltage only for a desired period, it is discharged in the 0V through an N-MOS transistor being connected to it. As a feeder of a non-selection block is always actuated in the 0V, a subthreshold current is not made to flow through the word driver in the non-selection block. Accordingly, the whole through current is significantly decreased to one piece of a through current only in roughly a selection block.



F-2075

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審査請求　未請求　請求項の数２　ＯＬ　（全　３　頁）

(21)出願番号　特願平4－186989

(22)出願日　平成４年(1992)７月14日

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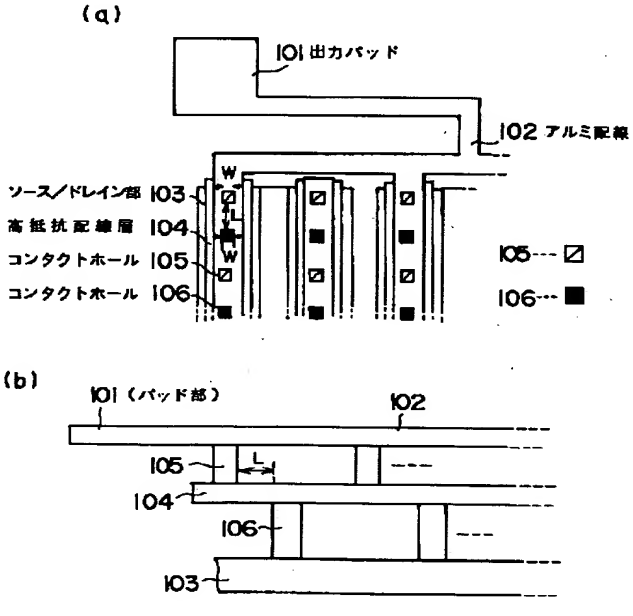
(54)【発明の名称】　半導体デバイスにおける静電破壊防止回路およびその形成方法

(57)【要約】

【目的】　静電気による電荷に対しては充分な電圧降下の抵抗分を保ちつつ、回路全体の配線抵抗を小さくし、チップサイズの縮小も可能とした半導体デバイスにおける静電破壊防止回路およびその形成方法を提供すること。

【構成】　シリコン単結晶半導体基板上に、出力トランジスタのソース／ドレイン部１０３を形成し、次に、高抵抗配線層１０４とトランジスタのソース／ドレイン部１０３とを接続させるコンタクトホール１０６をホトリソグラフィー／エッチング技術により開孔し、その後、高抵抗配線層１０４を形成する。そして、コンタクトホール１０５を開孔し、出力パッド１０１及びアルミ配線１０２を形成する。静電破壊防止回路としての電圧降下分の抵抗を得る構成要素としては、高抵抗配線層１０４のシート抵抗、コンタクトホール１０５，１０６の径、コンタクトホール１０３と１０４の間隔でありこれら３つの要素を組み合わせる。



静電破壊防止回路の実施例

【特許請求の範囲】

【請求項１】　出力端子に加わった静電気より内部回路を保護する半導体デバイスにおける静電破壊防止回路において、

出力トランジスタのソース／ドレイン部となる拡散層の上に、第１のコンタクトホールを介して静電気による電荷の電圧降下を行う高抵抗配線層を配置し、

前記高抵抗配線層の上に第２のコンタクトホールを介して前記出力端子と接続される金属配線を配置したことを特徴とする半導体デバイスにおける静電破壊防止回路。

【請求項２】　出力端子に加わった静電気より内部回路を保護する半導体デバイスにおける静電破壊防止回路の形成方法において、

トランジスタのソース／ドレイン部と高抵抗配線層を接続する第１のコンタクトホールを形成する工程と、

前記高抵抗配線層と出力端子に連結する金属配線とを接続する第２のコンタクトホールを形成する工程とを含み、

前記第１のコンタクトホールと第２のコンタクトホールとが互いに隣接し合うようにパターン形成されることを特徴とする半導体デバイスにおける静電破壊防止回路の形成方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は静電破壊防止回路、より具体的には半導体デバイスにおける出力端子側に設けられた保護回路に関する。

【０００２】

【従来の技術】図２は従来の半導体デバイスにおける静電破壊防止機能を有する出力保護回路の一構成例を示すもので、（ａ）は平面図、（ｂ）はその構成が理解しやすいように記載した断面図である。

【０００３】同図において、符号１はアルミニウム合金などで形成される出力パッド、符号２は出力端子とポリシリコンなどで形成される高抵抗配線３とを結ぶコンタクトホール、符号４はその高抵抗配線層３と出力トランジスタへとつながるアルミニウム配線５とを結ぶコンタクトホール、符号７はそのアルミニウム配線５とＮ型もしくはＰ型の不純物拡散層で形成される入力トランジスタのソース／ドレイン部６を結ぶコンタクトホールである。

【０００４】図２（ａ），（ｂ）の回路においては、出力パッド部１に静電気による電荷が印加された場合には出力トランジスタのソース・ドレイン間降伏により電流が流れるが、高抵抗配線層３による電圧降下によって出力トランジスタにかかるストレスを緩和させて、出力トランジスタを保護するというものであった。

【０００５】

【発明が解決しようとする課題】しかしながら、図２（ａ），（ｂ）の回路では、出力パッド１と出力トランジスタのソース／ドレイン部６との間に高抵抗配線層３が直列に接続されている。このため、高抵抗配線層３による配線抵抗分が大きくなり、デバイス全体の回路動作スピードが遅くなるという問題があった。また、高抵抗配線層３の占める面積が大きく、チップサイズの縮小化の妨げになるという問題があった。

【０００６】本発明はこのような配線抵抗が大きくなる問題点とチップサイズの縮小化の妨げになるという問題点を除去し、静電気による電荷に対しては充分な電圧降下の抵抗分を保ちつつ、回路全体の配線抵抗を小さくし、チップサイズの縮小も可能とした半導体デバイスにおける静電破壊防止回路およびその形成方法を提供することを目的とする。

【０００７】

【課題を解決するための手段および作用】本発明は上述の課題を解決するために、出力パッドに加わった静電気より内部回路を保護する半導体デバイスにおける静電破壊防止回路は、出力トランジスタのソース／ドレイン部となる拡散層の上に、第１のコンタクトホールを介して静電気による電荷の電圧降下を行う高抵抗配線層を配置し、高抵抗配線層の上に第２のコンタクトホールを介して出力パッドと接続される金属配線を配置した。

【０００８】また、本発明によれば、出力パッドに加わった静電気より内部回路を保護する半導体デバイスにおける静電破壊防止回路の形成方法は、トランジスタのソース／ドレイン部と高抵抗配線層を接続する第１のコンタクトホールを形成する工程と、高抵抗配線層と出力パッドに連結する金属配線とを接続する第２のコンタクトホールを形成する工程とを含み、第１のコンタクトホールと第２のコンタクトホールとが互いに隣接し合うようにパターン形成される。

【０００９】

【実施例】次に添付図面を参照して本発明による半導体デバイスにおける静電破壊防止回路およびその形成方法の実施例を詳細に説明する。

【００１０】図１（ａ），（ｂ）は、静電破壊防止回路の一実施例を示す平面図及びその概略断面図である。以下、これら図を参照して本実施例を説明する。

【００１１】まず、シリコン単結晶半導体基板上に、出力トランジスタのソース／ドレイン部１０３となるＮ型の不純物拡散層をヒ素などをイオン注入することにより形成する。その後、常圧ＣＶＤ法によりシリコン基板上にSiO_2膜を全面に生成させる。

【００１２】次に、高抵抗配線層１０４とトランジスタのソース／ドレイン部１０３とを接続させるコンタクトホール１０６をホトリソグラフィー／エッチング技術により開孔させる。

【００１３】その後、例えば減圧ＣＶＤ法によりポリシリコンを堆積させてヒ素などのイオン注入を行い、このポリシリコン膜の抵抗を調整し、ホトリソグラフィー／

エッチング技術により高抵抗配線層１０４を形成する。

【００１４】次に再び常圧ＣＶＤ法により、SiO_2 膜を堆積させる。その後、出力パッド１０１から続いているアルミ配線１０２と先述した高抵抗配線層１０４とを接続するコンタクトホール１０５をホトリソグラフィー／エッチング技術により開孔する。その後スパッタ法などによりアルミニウムを堆積させ、ホトリソグラフィー／エッチング技術により出力パッド１０１及びアルミ配線１０２を形成する。

【００１５】ここで従来の回路と同等な電圧降下分の抵抗を得る構成要素としては、（１）高抵抗配線層１０４のシート抵抗、（２）コンタクトホール１０５，１０６の径、（３）コンタクトホール１０３と１０４の間隔であり、これら３つの要素を適宜組み合わせて実現できる。

【００１６】なぜなら配線の抵抗ＲはＲ＝ρS ・Ｌ・Ｗで定義される。この場合、上述した（１）がρS 、（２）がＷ、（３）がＬに該当するからである。なお、図１にＬとＷの関係を図示した。

【００１７】コンタクトホール１０３及び１０４の組を増やせばＬ，Ｗ，ρS で決まる抵抗Ｒが、出力パッド１０１とトランジスタのソース／ドレイン部１０３の間でみるとそれだけ並列に入ることになり回路全体としては配線抵抗が小さくなるという効果を生む。

【００１８】またチップサイズの縮小化に関しては、図１（ａ）と図２（ａ）を比較して明らかなように、出力パッド１０１とアルミ配線１０２の間に高抵抗配線層が無いため、それだけ、パターンレイアウトを縮めることができる。

【００１９】

【発明の効果】このように本発明によれば、静電気による電荷の電圧降下に必要な高抵抗配線層を、アルミ配線とトランジスタのソース／ドレイン部となる拡散層との間に配置することにより、出力パッドからソース／ドレイン部までの抵抗がコンタクト間の配線抵抗の並列配置により小さくなる。また、出力パッドとアルミ配線の間に高抵抗配線層が不要となるため、回路の動作スピードが速くなり、かつチップ面積の縮小化が図れることが期待できる。

【図面の簡単な説明】

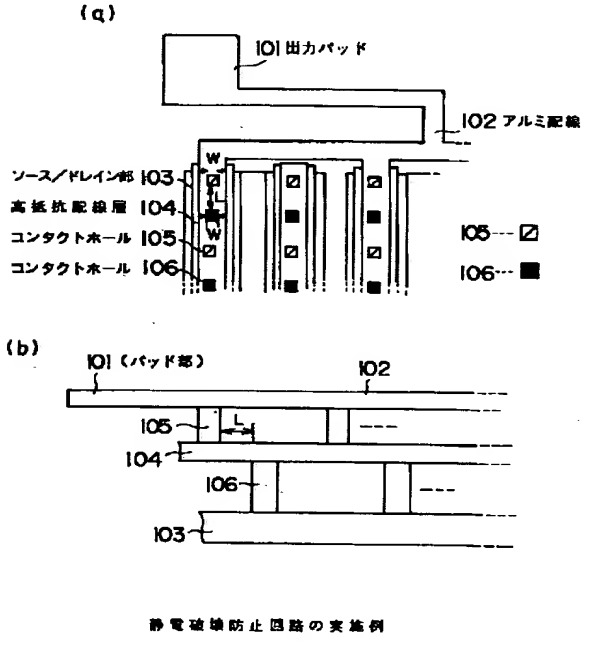
【図１】本発明の半導体デバイスにおける静電破壊防止回路の一実施例を示す平面及び断面。

【図２】従来の半導体デバイスの静電破壊防止回路である。

【符号の説明】

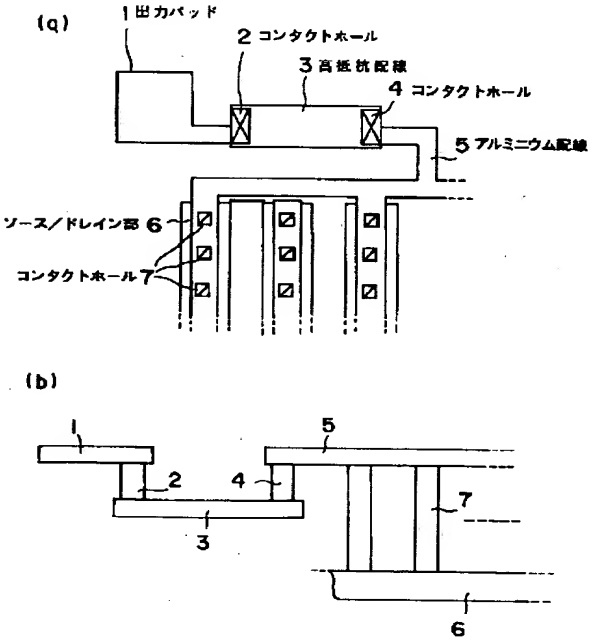
１０１	入力パッド
１０２	アルミ配線
１０３	トランジスタのソース／ドレイン部
１０４	高抵抗配線層
１０５，１０６	コンタクトホール

【図１】



静電破壊防止回路の実施例

【図２】



従来の静電破壊防止回路

PATENT ABSTRACTS OF JAPAN

(11)Publication number : **06-232345**
(43)Date of publication of application : **19.08.1994**

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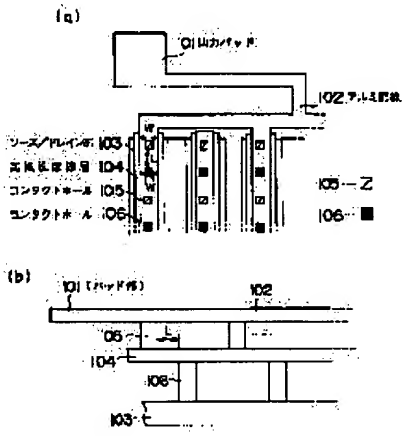
(21)Application number : **04-186989**
(22)Date of filing : **14.07.1992**

(71)Applicant : **OKI ELECTRIC IND CO LTD**
(72)Inventor : **ANDO HIDEYUKI**
KURACHI IKUO

(54) ELECTROSTATIC BREAKDOWN PREVENTIVE CIRCUIT IN SEMICONDUCTOR DEVICE AND FORMATION THEREOF

(57)Abstract:
PURPOSE: To provide an electrostatic breakdown preventive circuit in a semiconductor device of a structure, wherein while a sufficient resistance component of voltage drop to charge due to static electricity is kept, a wiring resistance in the whole circuit is made small and a reduction in a chip size is also made possible, and a method of forming the circuit.
CONSTITUTION: A source/drain part 103 of an output transistor is formed on a silicon single crystal semiconductor substrate, then, contact holes 106, which make, a high-resistance wiring layer 104 connect with the part 103 of the transistor, are opened by a photolithography/etching technique and after that, the layer 104 is formed. Contact holes 105 are opened and an output pad 101 and an at aluminum wiring 102 are formed. The constituent elements to obtain a resistance of a voltage drop component as an electrostatic breakdown preventive circuit are the sheet resistivity of the layer 104, the diameters of the contact holes 105 and 106 and the interval between the contact holes 103 and 104 and these three elements are combined with one another.



LEGAL STATUS

[Date of request for examination]	14.05.1998
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3128334
[Date of registration]	10.11.2000
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The electrostatic-discharge prevention circuit in the semiconductor device characterized by to have arranged the high resistance wiring layer which performs the voltage drop of the charge by static electricity through the 1st contact hole on the diffusion layer which serves as the source / drain section of an output transistor from static electricity which joined the output terminal in the electrostatic-discharge prevention circuit in the semiconductor device which protects an internal circuitry, and to have arranged the metal wiring connected with the aforementioned output terminal through the 2nd contact hole at the aforementioned quantity resistance wiring layer top.
[Claim 2] In the formation method of the electrostatic-discharge prevention circuit in the semiconductor device which protects an internal circuitry from static electricity which joined the output terminal The process which forms the 1st contact hole which connects the source / drain section, and the high resistance wiring layer of a transistor, The process which forms the 2nd contact hole which connects the metal wiring connected with the aforementioned quantity resistance wiring layer and an output terminal is included. The formation method of the electrostatic-discharge prevention circuit in the semiconductor device characterized by carrying out pattern formation so that the 1st contact hole of the above and the 2nd contact hole may adjoin each other.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to an electrostatic-discharge prevention circuit and the protection network more specifically prepared in the output terminal side in a semiconductor device.
[0002]
[Description of the Prior Art] It is the cross section indicated that drawing 2 shows the example of 1 composition of the output protection network which has an electrostatic-discharge prevention function in the conventional semiconductor device, for a plan to understand (a) and the composition is easier to understand (b).
[0003] In this drawing, the output pad with which a sign 1 is formed by the aluminium alloy etc., the contact hole with which a sign 2 connects an output terminal and the high resistance wiring 3 formed with contest polysilicon etc., the contact hole which connects the aluminum wiring 5 with which a sign 4 is connected to the high resistance wiring layer 3 and output transistor, and a sign 7 are contact holes which connect the source / drain section 6 of the input transistor formed in the impurity-diffusion layer of the aluminum wiring 5 and N type, or P type.
[0004] In the circuit of drawing 2 (a) and (b), although current flowed by the breakdown between source drains of an output transistor when the charge by static electricity was impressed to the output pad section 1, by the voltage drop by the high resistance wiring layer 3, the stress concerning an output transistor is made to ease and the output transistor was protected.
[0005]
[Problem(s) to be Solved by the Invention] However, in the circuit of drawing 2 (a) and (b), the high resistance wiring layer 3 is connected in series between the output pad 1, and the source / drain section 6 of an output transistor. For this reason, there was a problem that the amount of [by the high resistance wiring layer 3] wiring resistance became large, and the circuit operation speed of the whole device became slow. Moreover, there was a problem that the area which the high resistance wiring layer 3 occupies was large, and became the hindrance of reduction-izing of a chip size.
[0006] It aims at offering the electrostatic-discharge prevention circuit in the semiconductor device which made wiring resistance of the whole circuit small and also enabled reduction of a chip size, and its formation method, removing the trouble that this invention becomes the hindrance of reduction-izing of the trouble that such wiring resistance becomes large, and a chip size, and maintaining a resisted part of sufficient voltage drop to the charge by static electricity.
[0007]
[Means for Solving the Problem and its Function] In order that this invention may solve an above-mentioned technical problem, the electrostatic-discharge prevention circuit in the semiconductor device which protects an internal circuitry from static electricity which joined the output pad has arranged the high resistance wiring layer which performs the voltage drop of the charge by static electricity through the 1st contact hole on the diffusion layer used as the source / drain section of an output transistor, and has arranged the metal wiring connected with an output pad through the 2nd contact hole on a high resistance wiring layer.
[0008] According to this invention, moreover, the formation method of the electrostatic-discharge prevention circuit in the semiconductor device which protects an internal circuitry from static electricity which joined the output pad The process which forms the 1st contact hole which connects the source / drain section, and the high resistance wiring layer of a transistor, Including the process which forms the 2nd contact hole which connects the metal wiring connected with a high resistance wiring layer and an output pad, pattern formation is carried out so that the 1st contact hole and 2nd contact hole may adjoin each other.
[0009]
[Example] Next, with reference to an accompanying drawing, the example of the electrostatic-discharge prevention circuit in the semiconductor device by this invention and its formation method is explained in detail.
[0010] Drawing 1 (a) and (b) are the plan showing one example of an electrostatic-discharge prevention circuit, and its outline cross section. Hereafter, this example is explained with reference to these views.
[0011] First, the impurity diffusion layer of N type used as the source / drain section 103 of an output transistor is formed by carrying out the ion implantation of the arsenic etc. on a silicon-single-crystal semiconductor substrate. Then, it is SiO2 on a silicon substrate by ordinary-pressure CVD. The whole surface is made to generate a film.
[0012] Next, the contact hole 106 to which the high resistance wiring layer 104, and the source / drain section 103 of a

transistor are connected is made to puncture with phot lithography / etching technology.
[0013] Then, for example, contest polysilicon is made to deposit by reduced pressure CVD, which arsenic ion implantation is performed, resistance of this polysilicon contest film is adjusted, and the high resistance wiring layer 104 is formed with phot lithography / etching technology.
[0014] Next, it is SiO2 by ordinary-pressure CVD again. A film is made to deposit. Then, the contact hole 105 which connects the high resistance wiring layer 104 which carried out point ** with the aluminum wiring 102 which continues from the output pad 101 is punctured with phot lithography / etching technology. Aluminum is made to deposit by the spatter etc. after that, and the output pad 101 and the aluminum wiring 102 are formed with phot lithography / etching technology.
[0015] As a component which obtains resistance for a voltage drop equivalent to the here conventional circuit, it is sheet resistance of the (1) high resistance wiring layer 104, the path of the (2) contact hole 105,106, and the interval of the (3) contact holes 103 and 104, and can realize, combining these three elements suitably.
[0016] Because, the resistance R of wiring is defined by R=rho S and L-W. In this case, (1) mentioned above is because rhoS and (2) correspond to W and (3) corresponds to L. In addition, the relation between L and W was illustrated to drawing 1 .
[0017] If the group of contact holes 103 and 104 is increased, they will be L, W, and rhoS. If the decided resistance R sees between the output pad 101, and the source / drain section 103 of a transistor, it will enter so in parallel and the effect that wiring resistance becomes small as the whole circuit will be induced.
[0018] Moreover, since drawing 1 (a) is compared with drawing 2 (a), and there is no high resistance wiring layer between the output pad 101 and the aluminum wiring 102 about reduction-izing of a chip size so that clearly, a pattern layout can be contracted so much.
[0019]
[Effect of the Invention] Thus, according to this invention, resistance from an output pad to the source / drain section becomes small by the parallel arrangement of the wiring resistance during contact by arranging a high resistance wiring layer required for the voltage drop of the charge by static electricity between the diffusion layers used as aluminum wiring, and the source / drain section of a transistor. Moreover, since a high resistance wiring layer becomes unnecessary between an output pad and aluminum wiring, it is expectable that a speed of a circuit of operation becomes quick, and reduction-ization of chip area can be attained.

[Translation done.]

* NOTICES *

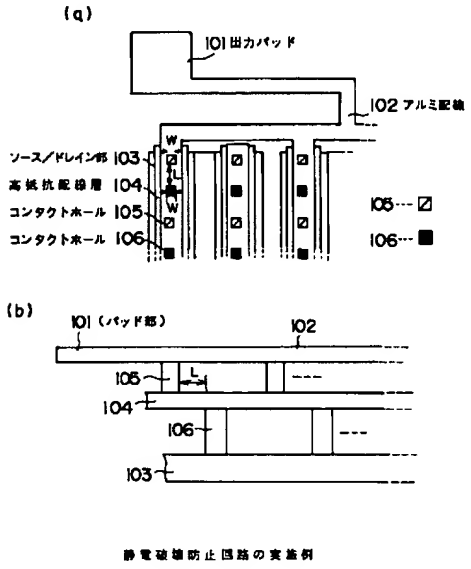
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The flat surface and cross section which show one example of the electrostatic-discharge prevention circuit in the semiconductor device of this invention.
[Drawing 2] It is the electrostatic-discharge prevention circuit of the conventional semiconductor device.
[Description of Notations]
101 Input Pad
102 Aluminum Wiring
103 Source / Drain Section of Transistor
104 High Resistance Wiring Layer
105,106 Contact hole

[Translation done.]

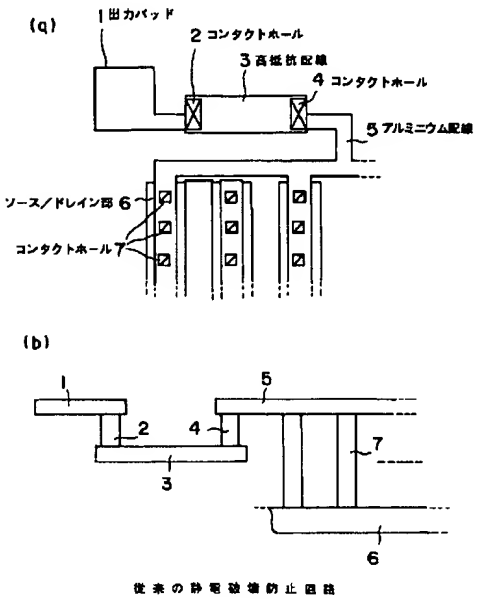
Drawing selection drawing 1



静電破壊防止回路の実施例

[Translation done.]

Drawing selection drawing 2



従来の静電破壊防止回路

[Translation done.]